## REMARKS

Prior to the present response, claims 1, 6-8, 14-16, and 19-20 were pending in the present application, and remain pending in the present application. Withdrawal of the present final rejection and reexamination and allowance of pending claims 1, 6-8, 14-16, and 19-20 in view of the following remarks are respectfully requested.

### A. Rejection of Claims Under 35 USC §103(a)

The Examiner has rejected original claims 1, 6-8, and 14-16, and 19-20 under 35 USC §103(a) as being unpatentable over U.S. Patent Application Publication No. 2005/0079696 to Colombo (hereinafter "Colombo") in view of U.S. Patent No. 6,265,260 to Alers et al. (hereinafter "Alers"), or U.S. Patent No. 6,566, 250 to Tu et al. (hereinafter "Tu") as evidenced by U.S. Patent Application Publication No. 2004/0188240 to Change et al. (hereinafter "Chang '240"), or U.S. Patent No. 6,090,210 to Ballance et al. (hereinafter "Ballance"), or U.S. Patent No. 6,759,337 to Aronowitz et al. (hereinafter "Aronowitz"), or U.S. Patent Application Publication No. 2005/0019964 to Change et al. (hereinafter "Chang '964"). The Examiner has withdrawn the previous rejections based on U.S. Patent No. 6,162,717 to Yeh (hereinafter "Yeh"). For the reasons that follow, Applicant submits that the present invention, as defined by amended independent claims 1, 8, and 15, is patentably distinguishable over the cited references, either singly or in combination.

By reference to Figures 1 and 2 of the present application, the present invention performs a nitridation process on gate stack 102 immediately after the gate etch process has been performed. By performing the nitridation process to nitridate sidewalls 110 of gate stack 102 after the gate etch process has been performed, the present invention's process flow can utilize the nitridation process to repair damage that may occur to gate stack 102 during the gate etch process. Additionally, during the nitridation process, nitrogen is introduced into high-k dielectric segment 106. As a result, the nitrogen that is introduced into high-k dielectric segment 106 can form a barrier that can prevent undesirable lateral oxygen diffusion into high-k dielectric segment 106 during subsequent processing steps. In an embodiment of the present invention that utilizes a gate stack comprising an interfacial layer, where the interfacial layer comprises nitride, the nitridation process can also replace nitride that has been depleted in the interfacial layer during the gate etch process. *See, e.g., page 8 of the present application, lines 9-21.* Moreover, as required by the independent claims, the processes of etching the gate stack and the nitridation of the etched gate stack are performed in a single process chamber. *See, e.g., page 9 of the present application, lines 20-22.* Utilization of a single process chamber has a number of advantages; for example, there will be no need to break vacuum and, thus, throughput is increased and manufacturing costs are reduced.

Colombo describes an encapsulated MOS transistor gate structures and methods for making the same. According to Colombo, sidewalls of patterned gate structures are conditioned by nitriding the sidewalls of the gate structure, and a silicon nitride

encapsulation layer is formed to protect the conditioned sidewalls during manufacturing processing. The conditioning and encapsulation avoid oxidation of metal gate layers, and also facilitate repairing or restoring stoichiometry of metal that may be damaged or altered during gate patterning. *See, Figures 4, and 5G through 5L of Colombo.*

However, as the Examiner has acknowledged, Colombo does not teach, disclose, or suggest utilizing plasma, much less using the same plasma chamber for both the gate etch and nitridation processes as disclosed and claimed by the present invention. *See, e.g., page 4 of the present Office Action, lines 5-7.* However, the Examiner has stated that any of the cited references Alers or Tu can be used to cure this deficiency of Colombo, as evidenced by Chang '240, Ballance, Aronowitz, or Chang '964. *See, e.g., page 3 of the present Office Action, lines 12-17.*

Alers is directed to a method for making a capacitor by forming a first metal electrode comprising a metal nitride surface and a tantalum pentoxide layer on the metal nitride surface while maintaining a temperature below an oxidizing temperature of the metal, and remote plasma annealing the tantalum pentoxide layer. *See, e.g., column 1, line 62 through column 2, line 54 of Alers.* Thus, Alers does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch.

Moreover, Tu is directed to forming a self-aligned capping layer over a metal filled feature in a semiconductor device by blanket deposition of a first barrier layer over an anisotropically etched feature to prevent diffusion of metal into the substrate; filling the

anisotropically etched feature with a metal to form a metal filled feature; planarizing the substrate surface to form an exposed surface of the metal filled feature; and depositing a second barrier layer to cover the exposed surface of the metal filled feature to form a capping layer. *See, e.g., column 3, lines 37-53 of Tu.* Thus, Tu does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch.

Further, Chang '240 is directed to a process for the in-situ nitridation and formation of metal salicides. Change '240 discloses accomplishing its objective to form metal salicides by utilizing a plasma generator. However, Chang'240 does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch.

Ballanace discloses utilizing a "showerhead" for accomplishing a multi-zone gas flow control into a substrate in a process chamber. In accomplishing this objective, Ballance discloses a first gas distribution system which delivers a first gas to a first subset of injection ports for injection into the chamber, and a second gas distribution system which delivers a second gas to a second subset of injection ports for injection into the chamber. However, Ballance does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch.

Aronowitz discloses a process where a uniform amount of silicon oxide can be removed from a surface of an oxide previously formed over a semiconductor substrate by exposing the oxide to a nitrogen plasma in an etch chamber while applying an RF bias to the substrate support

in the etch chamber. However, Aronowitz does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch.

Moreover, Chang '964 discloses a method for determining a composition of an integrated circuit feature on a substrate, including collecting intensity data representative of spectral wavelengths of radiant energy generated by a plasma during plasma nitridation of the integrated circuit feature on the substrate, and analyzing the intensity data to determine a peak intensity at one of the wavelengths. However, Chang '964 does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch. Thus, independent claims 1, 8 and 15 are patentably distinguishable over each primary reference Colombo, Alers, or Tu singly, or in any of their respective combinations with secondary references Chang '240, Ballance, Aronowitz, or Chang '964.

**B. Rejection of Claims Under 35 USC §103(a)**

The Examiner has rejected original claims 1, 6-8, and 14-16, and 19-20 under 35 USC §103(a) as being unpatentable over U.S. Patent No. 5,891,798 to Doyle et al. (hereinafter "Doyle") in view of Alers or Tu as evidenced by Chang '240, or Ballance, or Aronowitz, or Chang '964. For the reasons that follow, Applicant submits that the present invention, as defined by amended independent claims 1, 8, and 15, is patentably distinguishable over the cited references, either singly or in combination.

Doyle discloses a method for increasing the dielectric constant of a gate dielectric by using a high dielectric constant material, such as a paraelectric material, instead of

silicon dioxide. First, nitrogen is implanted into the silicon through a sacrificial oxide layer. After annealing the substrate and stripping the sacrificial oxide, a dielectric layer is formed from a material with a high dielectric constant, such as a paraelectric material. Although the paraelectric material provides a source of oxygen for oxidation of silicon in subsequent high temperature process steps, Doyle claims that no oxidation takes place due to the presence of the nitrogen in the silicon. Therefore, there is no undesired decrease in the overall capacitance of the dielectric. When a gate electrode is formed on the dielectric layer, a nitrogen implant into the gate electrode can be used to prevent oxidation at the upper interface of the gate dielectric. *See, e.g., column 2, line 48 through column 3, line 44 of Doyle.* However, Doyle does not suggest that the processes of etching the gate stack and the nitridation of the etched gate stack are performed in a single plasma chamber. Moreover, as discussed above, use of a single plasma nitridation process chamber is not suggested by Alers or Tu, or their combination with Chang '240, Ballance, Aronowitz, or Chang '964. Thus, independent claims 1, 8 and 15 are patentably distinguishable over each primary reference Alers or Tu singly, or in any of their respective combinations with secondary references Chang '240, Ballance, Aronowitz, or Chang '964.

### C. Conclusion

For the foregoing reasons, independent claims 1, 8, and 15 are patentably distinguishable over the cited art. Moreover, the pending dependent claims are also

distinguishable over the cited art for the reasons discussed above and also for additional limitations contained in each dependent claim. Thus, it is submitted that all claims 1, 6-8, 14-16, and 19-20 remaining in the present application are in condition for allowance, and withdrawal of the finality of rejection and an early notice of allowance directed to all pending claims 1, 6-8, 14-16, and 19-20 are respectfully requested.

Attorney Docket No.: 0180151

Respectfully Submitted,
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Date: 2/6/06

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